Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **INPUT A**
2. **INPUT B**
3. **QA**
4. **QB**
5. **QC**
6. **QD**
7. **GND**
8. **CLOCK**
9. **CLEAR**
10. **QE**
11. **QF**
12. **QG**
13. **QH**
14. **VCC**

**.075”**

**.067”**

**13**

**14**

**1**

**2**

**3 4 5 6**

**9**

**8**

**7**

**12 11 10**

**LS**

**164**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: LS164**

**APPROVED BY: DK DIE SIZE .067” X .075” DATE: 8/29/22**

**MFG: TEXAS INSTRUMENTS THICKNESS .015” P/N: 54LS164**

**DG 10.1.2**

#### Rev B, 7/1